AMENDMENTS TO THE CLAIMS:

Please cancel without prejudice claims 5 and 18 and amend claims 1, 2, 14 and 15 as follows.

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) Apparatus for processing data, said apparatus comprising:

a processor configured to perform processing operations under control of program instructions;

a stack data store configured to store one or more sets of state data, each set associated with a respective processing performed by said processor when an interrupt event occurs, each said interrupt event is associated with a ~~programmable~~ priority ~~level~~that is programmable both before and after said interrupt event occurs; and

an interrupt controller, in response to a first interrupt event, for ~~saving~~storing to said stack data store first state data associated with processing being performed when said first interrupt event occurred and for redirecting program instruction execution to a first interrupt handling program and, upon completion of said first interrupt handling program, for detecting if one or more second interrupt events having a higher priority than said processing that was interrupted by said first interrupt event has occurred during execution of said first interrupt handling program and

(i) if said one or more second interrupt events has occurred, then redirecting program instruction execution to a second interrupt handling program without saving further state data to said stack data store; and

(ii) if said one or more second interrupt event has not occurred, then reloading said first state data from said stack data store and resuming said processing that was interrupted by said first interrupt event, wherein when said stack data store is storing a plurality of sets of state data, each set associated with a respective one of a plurality of interrupt events, said interrupt controller is further configured to determine a stack priority level corresponding to the highest priority interrupt event among ~~the~~said plurality of interrupt events associated with said ~~one or more~~plurality of sets of state data stored in said stack data store; and

said interrupt controller is further configured to detect that said one or more second interrupt events have a higher priority than said processing that was interrupted by said first interrupt event if said one or more second interrupt event has a higher priority than said stack priority level.

2. (currently amended) Apparatus as claimed in claim 1, wherein said first state data includes one or more of:

a program counter value corresponding to a current program execution point;

a processor status register value corresponding to one or more state variables of said apparatus; and

one or more data processing register values corresponding to data values held within at least some general purpose data processing registers of said apparatus.

3. (original) Apparatus as claimed in claim 1, wherein said processing being performed when said first interrupt event occurred was one of:

execution of a non-interrupt triggered program; and

execution of an active interrupt handling program, said interrupt controller being a nested interrupt controller permitting a pending interrupt handling program to pre-empt said active interrupt handling program if said active interrupt handling program has a lower priority than said pending interrupt handling program.

4. (original) Apparatus as claimed in claim 1, wherein said first interrupt event and said one or more second interrupt events each have respective priority values, said interrupt controller being operable to compare said respective priority values to determine if any of said one or second interrupts event has a higher priority than said first interrupt event and if so to pre-empt execution of said first interrupt handling program with execution of said a second interrupt handling program.

5. (cancelled).

6. (original) Apparatus as claimed in claim 1, wherein said interrupt controller is responsive to a late interrupt signal during reloading of said first state data to abort a return to said processing being performed when said first interrupt event occurred and instead redirect execution to an interrupt handling program associated with said late interrupt signal.

7. (original) Apparatus as claimed in claim 1, wherein if such a said second interrupt event has occurred, then redirection of program instruction execution to said second interrupt handling program occurs without reloading said first state data from said stack data store.

8. (original) Apparatus as claimed in claim 6, wherein upon aborting said return, said stack data store is repaired to undo any alterations made by partial completion of said return.

9. (original) Apparatus as claimed in claim 8, wherein said repair includes repairing one or more of stack pointer data and link register data.

10. (original) Apparatus as claimed in claim 1, wherein transfer of data values to said stack data store under control of said interrupt controller is performed in parallel with and asynchronously to loading of program counter location and program instructions into an instruction pipeline prior to execution.

11. (original) Apparatus as claimed in claim 1, wherein said interrupt controller is responsive to execution of a return instruction with a predetermined link address value loaded within a link register to perform a return from interrupt operation.

12. (original) Apparatus as claimed in claim 1, wherein said stack data store is a stack memory.

13. (original) Apparatus as claimed in claim 1, wherein when there are no pending interrupts said apparatus enters a low power mode in which processing is halted awaiting an interrupt event.

14. (currently amended) A method of processing data, said method comprising the steps of:

performing processing operations under control of program instructions;

~~saving~~storing to a stack data store one or more sets of state data, each set associated with a respective processing performed when an interrupt event occurs, each ~~of~~ said interrupt events is associated with a ~~programmable~~ priority ~~level~~that is programmable both before and after said interrupt event occurs; and

in response to a first interrupt event, ~~saving~~storing to said stack data store first state data associated with processing being performed when said first interrupt event occurred and to redirect program instruction execution to a first interrupt handling program, wherein upon completion of said first interrupt handling program, detecting if a second interrupt event having a higher priority than said processing that was interrupted by said first interrupt event has occurred during execution of said first interrupt handling program and

(i) if said second interrupt event has occurred, then redirecting program instruction execution to a second interrupt handling program without saving further state data to said stack data store; and

(ii) if said second interrupt event has not occurred, then reloading said first state data from said stack data store and resuming said processing that was interrupted by said first interrupt event, wherein when said stack data store is storing a plurality of sets of state data, each set associated with a respective one of a plurality of interrupt events, said detecting step includes a step of determining a stack priority level corresponding to the highest priority interrupt event among ~~the~~said plurality of interrupt events associated with said ~~one or more~~ plurality of sets of state data stored in said stack data store; and

said detecting step detects that said one or more second interrupt events have a higher priority than said processing that was interrupted by said first interrupt event if said one or more second interrupt event has a higher priority than said stack priority level.

15. (currently amended) A method as claimed in claim 14, wherein said first state data includes one or more of:

a program counter value corresponding to a current program execution point;

a processor status register value corresponding to one or more state variables of an apparatus perform said method; and

one or more data processing register values corresponding to data values held within at least some general purpose data processing registers of said apparatus.

16. (original) A method as claimed in claim 14, wherein said processing being performed when said first interrupt event occurred was one of:

execution of a non-interrupt triggered program; and

execution of an active interrupt handling program, interrupt control being nested interrupt control permitting a pending interrupt handling program to pre-empt said active interrupt handling program if said active interrupt handling program has a lower priority than said pending interrupt handling program.

17. (original) A method as claimed in claim 14, wherein said first interrupt event and said second interrupt event each have respective priority values, said respective priority values being

compared to determine if said second interrupt event has a higher priority than said first interrupt event.

18. (cancelled).

19. (original) A method as claimed in claim 14, wherein in response to a late interrupt signal during reloading of said first state data, aborting a return to said processing being performed when said first interrupt event occurred and instead redirecting execution to an interrupt handling program associated with said late interrupt signal.

20. (original) A method as claimed in claim 14, wherein if such a said second interrupt event has occurred, then redirection of program instruction execution to said second interrupt handling program occurs without reloading said first state data from said stack data store.

21. (original) A method as claimed in claim 19, wherein upon aborting said return, said stack data store is repaired to undo any alterations made by partial completion of said return.

22. (original) A method as claimed in claim 21, wherein said repair includes repairing one or more of stack pointer data and link register data.

23. (original) A method as claimed in claim 14, wherein transfer of data values to said stack data store is performed in parallel with and asynchronously to loading of program counter location and program instructions into an instruction pipeline prior to execution.

24. (original) A method as claimed in claim 14, wherein in response to execution of a return instruction with a predetermined link address value loaded within a link register, performing a return from interrupt operation.

25. (original) A method as claimed in claim 14, wherein said stack data store is a stack memory.

26. (original) A method as claimed in claim 14, wherein when there are no pending interrupts a low power state is entered in which processing is halted awaiting an interrupt event.